REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application and for properly making this third Official Action non-final. Arguments supporting patentability of the claims are presented in detail below.

I. The Claimed Invention

The present invention, as recited in independent Claim 25, for example, is directed to a process for fabricating an integrated circuit comprising forming a gate on a silicon substrate, and implanting dopants in the silicon substrate to form drain and source extensions therein. The process also comprises amorphizing regions of the silicon substrate to obtain amorphous silicon regions adjacent the gate after implanting the dopants. The process further comprises forming drain and source regions in the respective drain and source extensions with a channel being defined therebetween with the drain and source regions being formed at a temperature below 800°C.

Independent Claim 54 is similar to Claim 25, but instead of the temperature recitation of less than 800 C, Claim 54 recites the drain and source regions being formed at a relatively low temperature to avoid diffusion of the dopants from the drain and source extensions.

II. The Wierczorek et al. patent Is Not Prior Art

The Examiner rejected independent Claims 25 and 54 over the Pramanick et al. patent in view of the Wierczorek et al. patent. The Wierczorek et al. patent has a priority date

of December 23, 2002. The priority date of the present application is November 14, 2002.

The Examiner cited the Pramanick et al. patent as disclosing all of the elements recited in the independent claims except for the drain and source regions being formed at a temperature below 800°C. The Examiner cited the Wierczorek et al. patent as disclosing a field effect transistor with the drain and source regions being formed at a temperature below 800°C. Since the Wierczorek et al. patent is not prior art, and the Examiner correctly notes that Pramanick et al. patent fails to disclose that the drain and source regions are formed at a temperature below 800°C, the Applicant submits that the claims are patentable.

III. The Claims Are Patentable

Even if the Wierczorek et al. patent was prior art, the claims are still patentable. In particular, the Examiner rejected independent Claims 25 and 54 over the Pramanick et al. patent in view of the Wierczorek et al. patent. The Pramanick et al. patent is directed to a method for achieving shallow junctions by providing an amorphous silicon layer. In the Pramanick et al. patent, germanium or silicon ion is implanted to form amorphous silicon layer regions **22, 23** as shown in FIG. 1. A gate oxide **24** is formed as shown in FIG. 2. The amorphous silicon layer regions **22, 23** are annealed at a temperature of 800°C for a time period of 40 seconds causing the dopant to activate to form shallow, lightly doped source and drain regions **30, 32** as shown in FIG. 3. During the anneal step, the amorphous silicon layer regions **22, 23**

recrystallize, thus growing the entire lattice up from the remaining monocrystalline silicon layer **12**.

As correctly noted by the Examiner, the Pramanick et al. patent fails to disclose forming the drain and source regions at a temperature below 800°C, as in the claimed invention. The Examiner cited the Wierczorek et al. patent as disclosing a field effect transistor with the drain and source regions being formed at a temperature below 800°C. The Examiner has taken the position that it would have been obvious to form the drain and source regions in the Pramanick et al. patent at a temperature below 800°C based upon the Wierczorek et al. patent in order to obtain better performance.

It appears that the Examiner is using impermissible hindsight to produce the claimed invention. Moreover, it is also respectfully submitted that there can be no proper motivation or suggestion to combine the prior art as the Examiner proposes, since doing so would likely render the Pramanick et al. patent unsatisfactory for its intended purpose. In the Pramanick et al. patent, the monocrystalline silicon layer **12** is grown on a silicon substrate **10**, and germanium or silicon ions are implanted into the monocrystalline silicon layer **12** to form the amorphous silicon layer regions **22**, **23**. Reference is directed to column 2, lines 57-60 of the Pramanick et al. patent, which provides:

> "Next, the resulting structure is annealed at, for example, a temperature of 800°C for a time period of 40 seconds (FIG. 3), causing the dopant to activate to form shallow, lightly doped source and drain regions **30**, **32**." (Emphasis added).

Since the monocrystalline silicon layer **12** is formed on the silicon substrate **10**, the Pramanick et al. patent discloses that the anneal is at a temperature of 800°C to form the source and drain regions **30, 32**. Consequently, annealing the structure at a temperature of less than 800°C may not form the source and drain regions **30, 32**.

Accordingly, it is submitted that independent Claim 25 is patentable over the Pramanick et al. patent in view of the Wierczorek et al. patent. Independent Claim 54 is similar to independent Claim 25. Therefore, it is submitted that these claims are also patentable over the Pramanick et al. patent in view of the Wierczorek et al. patent. In view of the patentability of independent Claims 25 and 54, it is submitted that their dependent claims, which recite yet further distinguishing features of the invention, are also patentable. These dependent claims require no further discussion herein.

IV. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,

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